

iMiD 2026

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Exhibitor Introduction	Silvaco is a provider of software solutions for semiconductor and photonics design, including TCAD, EDA software, and SIP solutions that enable semiconductor design and digital twin modeling through AI software and innovation. The company's innovative software and IP is used for the development of complex semiconductor and photonics processes, devices and systems across a variety of market segments, including display, power devices, automotive, memory, high-performance computing, foundries, photonics, IoT, and 5G/6G mobile markets. We offer a wide range of solutions as well as support for engineers and researchers worldwide. Our expertise covers a broad range of semiconductor design, from simulating devices at the atomic level to designing and analyzing transistor-level circuits and providing semiconductor IP blocks and creation tools for advanced SoC designs.	
Exhibit Description	Victory Process is a general-purpose layout driven 1D, 2D and 3D process and stress simulator including etching, deposition, implantation, diffusion, oxidation and stress simulation capabilities. Victory Device is a general-purpose 3D device simulator. A tetrahedral	

	meshing engine is used for fast and accurate simulation of complex 3D geometries. Victory Device performs DC, AC, and transient analysis for silicon, binary, ternary, and quaternary material-based devices. Gateway supports flat or hierarchical designs of any technology. Gateway readily accepts legacy designs from other schematic editors through OA and EDIF import. SmartSpice delivers the performance and accuracy required to design complex high precision analog circuits, analog mixed-signal circuits, analyze critical nets, characterize cell libraries, etc. SmartSpice is compatible with popular analog design flows and foundry-supplied device models. Expert is a high-performance hierarchical IC layout editor with full editing features, large capacity and fast layout viewing. Expert provides high level of design assistance with Schematic Driven Layout and parameterized cells (Pcells). SmartDRC and SmartLVS with SmartRDE deliver physical verification of analog, mixed signal, and RF IC designs with high performance and accuracy. Tightly integrated with Silvaco's schematic capture and layout editor, SmartDRC/LVS efficiently performs design rule checks (DRC), electrical rule checks (ERC), layout vs. layout comparison (LVL), fill layer generation, layout netlist extraction, and layout vs. schematic (SmartLVS) comparisons.
Exhibit Product	Victory TCAD Process & Device Simulation Gateway Schematic Editor, SmartSpice Circuit Simulator Expert Layout Editor